ABSTRACT

A CMOS circuit including a P-channel pull-up transistor (MP) and an N-channel pull-down transistor (MN) includes a first feedback circuit (6) producing a first delayed signal (V_7) on the gate of the pull-down transistor (MN) to turn on the pull-down transistor (MN) a first predetermined amount of time after the pull-up transistor (MP) is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor (MP) and the pull-down transistor (MN) and a second feedback circuit (4) producing a second delayed signal (V_5) on the gate of the pull-up transistor (MP) to turn on the pull-up transistor (MP) a second predetermined amount of time after the pull-down transistor (MN) is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor (MP) and the pull-down transistor (MN).